

Effect of a Non-Tight Constructions of DC-Link and Damping Oscillation to Improve the Efficiency of Fly-back Converter

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Abstract—This paper deals with improvement of the efficiency of fly-back converter that was used in traction drives application. There are lots of researches in this area and also some techniques to increase the performance of the converter. In this paper, the reference of the converter was modified in a non-tight construction of DC-Link and change the snubber circuit to reduce the damping oscillation. The result of performance the converter was simulated (theoretical) and measured. The result show that is changing the dc-link construction and snubber circuit improve the efficiency of the converter.

Index Terms—Fly-back converter, efficiency, damping oscillation, DC-link, snubber circuit

I. INTRODUCTION

The switching power supply system that have a high efficiency, reasonable size, good performance, and cheaper, is perfect power supply that can be used in a lots of area such as home appliance, telecommunication, manufacturing process, and others. The important part in the switching power supply that absorbs high losses is DC converter parts. Therefore, there are lots of researches to deals with improvement of efficiency the DC converter.

The DC converter efficiency can be increase by apply the active snubber network and eliminate the MOSFET output capacitance losses [1][2]. The most common technique to improve the efficiency of DC converter is by reduction of switching losses and increase operating frequency that has been recently widely applied [3]-[8]. Various soft-switched boost converters with active or passive snubber circuits have been proposed to increase the efficiency of DC Converter [9]-[13].

In this paper, a fly-back converter that was used in electric traction application will be used as reference. The converter was modified in the DC-link and changed the damping oscillation to improve an efficiency of fly-back converter. The comparison between simulation and measurement of this changing also investigate.

The paper is organized as follows: In the next section, brief reviews of switching losses are presented using Pspice Simulation software and the operation principle of converter are described. In Section III, a description of effect of a non tight construction of DC links in DC converter are simulated and measured. The next section, the effect of snubber circuit in damping oscillation are investigaed. Finally, the conclusions are made in next section.

II. SWITCHING LOSSES AND OPERATION PRINCIPLE OF FLY-BACK CONVERTER

In order to study the sources of losses, the operation is divided in several states. The losses corresponding to those occur in the following order: Switch-ON losses, On-state losses, Switch-OFF losses, OFF-state losses. The losses in the

switching component have been theoretically determined. Therefore the drain-source current and voltage have been simulated with a model using the software P-SPICE.

The result of fly-back converter is operating in discontinuous mode can be seen Fig. 1.

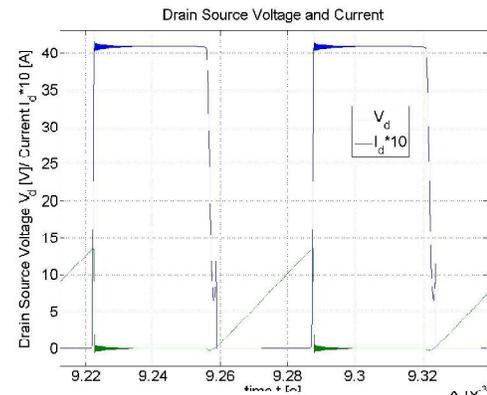


Fig. 1: Simulation - Drain Source Voltage and Current of the MOSFET

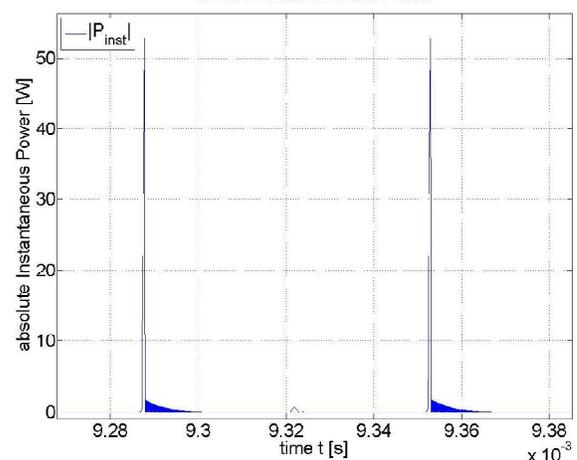


Fig. 2: Simulation - Instantaneous Power dissipation in the MOSFET

As shown in Fig. 2, there are different sources off losses during the period: the switching losses (switch-on, switch-off losses) and the state losses (on-state, off-state losses). The losses can be determined by integrating the instantaneous power over one period.

$$() = (1)$$

Whereas t_x represents the corresponding time interval for switch-on/off or on-state. The power losses averaged over one period are given by

$$= (2)$$

Knowing the switching frequency, the losses have been calculated for different sources of losses. The switching frequency is $f_s = 15.337$ kHz

The switching loss analysis can be simplified by neglecting the turn-on losses since the current in that state is approximately zero as can be seen from the simulation results in Fig. 1 and Fig. 2. The delay time t_{d_on} was neglected when estimating time t_{on} where the on-state begins. The power dissipation during the aforementioned state is relatively small in the simulations.

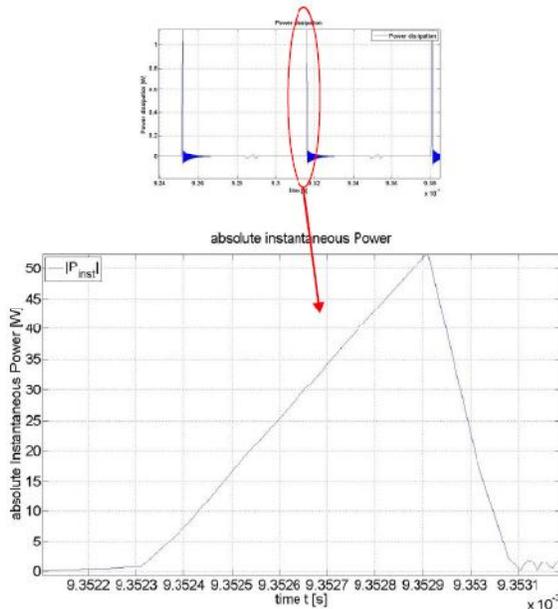


Fig. 3: Simulation - Instantaneous power at turn-off

Using (2) the energy $E_{switch-off}$ that is dissipated in the MOSFET during turn off is represented by the area under the curve shown in Fig. 3. The area can be approximated by the sum of a rectangular triangle and rectangle. The switch-on losses were neglected.

$$\approx (3)$$

The calculation can be done more accurately in Matlab summing up the samples of the instantaneous power in that are in the time interval $t_{coff} = t_2 - t_1$ (Fig. 3) as follows:

$$= * * = 0,284 (4)$$

where the time between two samples Δt_s was calculated by dividing t_{coff} with the number of samples lying in that space of time.

The following curves have been obtained from the oscilloscope were drawn and analyzed with MATLAB software.

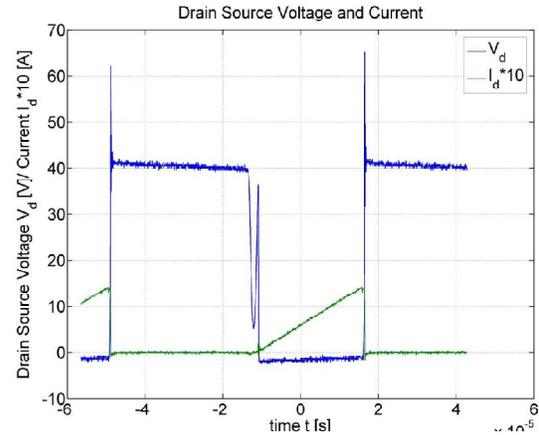


Fig. 4: Measured Drain Source Voltage and Current *10

As can be seen in Fig. 4 there are few oscillations in the drain source voltage as well as in the current compared with the simulation results.

It should be noted that the power losses in the on-state are much higher than in the simulation results (See Fig. 4 and Fig. 5). These are probably caused by noise [5].

The drain-source voltage is negative during the on-state since a zener diode operating reversed biased direction is connected anti-parallel with the drain source terminal. The zener diode keeps the drain source voltage of the MOSFET constant in the saturation region to use it as a switch only (avoiding operation in the linear region).

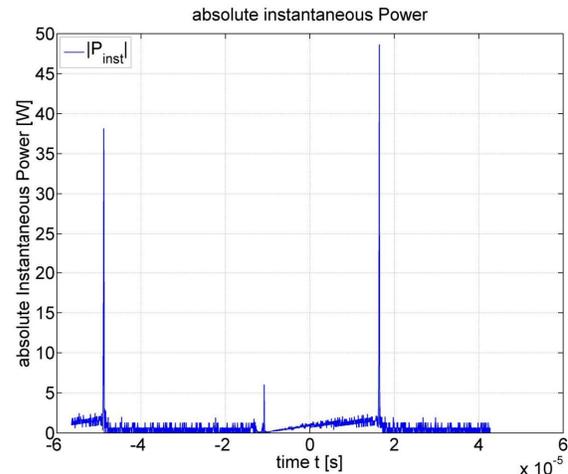


Fig. 5: Measurements - Calculated instantaneous power

In the same way as the loss calculations were done based on the simulation the measured quantities are loaded in the MATLAB file and the losses calculated. The losses at switch-on are still neglected approximating the switching losses with the switch-off losses are 0.0728W.

Proceeding in the same fashion with the determination of the on-state losses results in 0.399W.

The on-state losses contain a lot of high frequent components, caused by oscillations in the circuit and noise resulting in a higher value than in the simulation. As shown in Fig. 5 the losses in the off-state are not negligibly small. The latter one should be close to zero since there is a very small

current flow in the off-state. Considering the relatively high losses in the off-state one might conclude the high frequency components originate rather from noise than from inner oscillations on the circuit.

TABLE 1
COMPARISON OF LOSS DIFFERENT DETERMINATION (SIMULATED AND MEASURED)

	P_{ave} [W]	P_{cond} [W]	P_{on} [W]	P_{off} [W]	t_{off} [ms]	t_{on} [ms]	$I_{d_{rms}}$ [A]
Simulation	0.31	0.298	0.02	0.28	0.8	28.9	0.261
Measurement	0.73	0.472	0.4	0.07	0.34	28.5	0.564

Table 1 contains the power losses for the MOSFET in the original circuit setup for one period ($P_{average}$) as well as for the conduction interval consisting of the on-state ($P_{onstate}$) and switch-off interval ($P_{switch-off}$). For each phase the losses are given separately. There is a remarkable difference between the simulation and the measurement results:

The on-state losses calculated from the measured quantities are tremendously higher in comparison to those of the simulation, even though the on-state times are more or less equal for both the cases (See Table 1: $t_{onstate}$). This difference is caused by the high frequency components. Moreover the rms value of the current is remarkable higher for the measurement due to the contribution during the off-state which was negligibly small for the simulation. The results of the switch-off power also differ. Since the switch-off time t_{coff} is shorter for the real MOSFET than for the model the losses are lower in practice.

The switching losses are too high. In order to reduce the losses, several measures can be taken into consideration: adding a turn-off snubber, reducing the derivative of the drain source current dI_d/dt at rise and fall by adequately controlling the gate current, and reducing the switching frequency.

For the time being the losses should be reduced without making big changes on the circuit board. Hence the first and third point cannot be realized and only the second possibility is left-over. A reduction in the rise and fall time of the drain source current yields to lower power losses during switching: The area that is surrounded by the drain-source current and voltage curves is representing the dissipated energy. Consequently a reduction in that area results in a reduction of the switching loss.

The equivalent circuit of the MOSFET for the active region, which can be used for the transient analysis, is shown in Fig. 6.

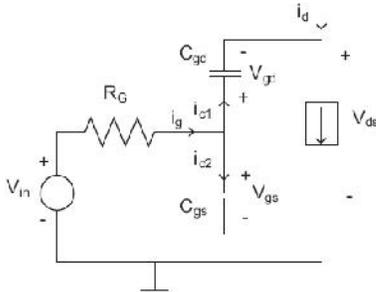


Fig. 6: Equivalent circuit of the MOSFET for the cut-off and active region
According to that circuit the gate current is determined by the drain-gate and gate-source capacitances as follows:

$$i_g = C_{gs} \frac{dV_{gs}}{dt} + C_{gd} \frac{dV_{gd}}{dt} \quad (5)$$

The variation of the drain-source voltage dependent capacitances C_{gs} and C_{gd} is small in the on-state, since the drain-source voltage V_{ds} is kept constant by the zener-diode. Another consequence of the constant drain-source voltage is:

$$\frac{dV_{gd}}{dt} = -\frac{dV_{ds}}{dt} \quad (6)$$

Thus if the gate current i_g can be increased, the gate-source and gate-drain voltage derivatives given in (6) and (5) will increase yielding to a shorter rise and fall time of the gate-source voltage. The drain current is a function of the aforementioned voltage:

$$i_d = \frac{V_{gs} - V_{th}}{R_g} + \beta (V_{gs} - V_{th})^2 \quad (7)$$

The objective is to maximize dI_D/dt which is given by

$$\frac{di_d}{dt} = \frac{1}{R_g} \frac{dV_{gs}}{dt} + 2\beta (V_{gs} - V_{th}) \frac{dV_{gs}}{dt} \quad (8)$$

At turn on the gate-source voltage is given by

$$V_{gs}(t) = V_{gs}(0) + \frac{V_{gs}(1) - V_{gs}(0)}{\tau} t \quad (9)$$

and at turn-off

$$V_{gs}(t) = V_{gs}(0) - \frac{V_{gs}(0) - V_{gs}(1)}{\tau} t \quad (9)$$

where τ is the time constant:

$$\tau = R_g (C_{gs} + C_{gd}) \quad (9)$$

As can be seen from (9) the time constant has to be decreased to maximize the derivative of $v_{gs}(t)$. Since the MOSFET capacitances cannot be changed, R_g is reduced. Considering the maximum output current of the drive circuit from the data sheet the minimum value for R_g that fulfills the constraint of $i_{g,max}=1A$.

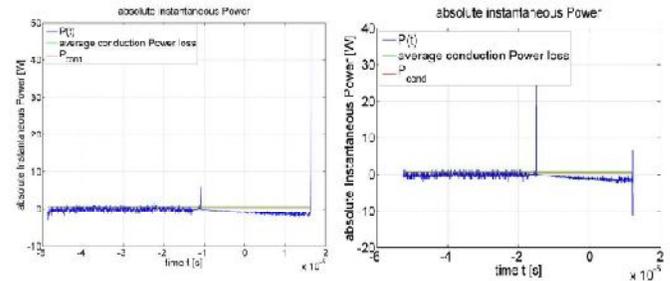


Fig. 7: Comparison of power losses before and after modification

The two curves above (Fig. 7) show the power losses during one switching period without the modified gate resistance (left) and after modification (right): As can be seen at the end of the period the switch off losses have tremendously been reduced. The calculation results from MATLAB are given in Table 2.

TABLE 2
COMPARISON OF LOSSES BEFORE AND AFTER MODIFYING THE GATE RESISTANCE R_g

	P_{ave} [W]	P_{cond} [W]	P_{on} [W]	P_{off} [W]	t_{off} [ms]	t_{on} [ms]	$I_{d_{rms}}$ [A]
Measurement	0.73	0.472	0.4	0.07	0.34	28.5	0.564
Measurement w/ new Rg	0.69	0.422	0.41	0.01	0.11	28.05	0.607
Deviation (%)	-4.8	-10.7	+2.7	-84	-	-	+7.6

The modification reduces the switch-off losses by 84%. Since the on-state interval is slightly longer the on-state losses $P_{onstate}$ increased with 2.7% as well as the rms value of the drain current $I_{d,rms}$ (+7.6%). The loss averaged over one period $P_{average}$ decreases with 4.8%.

III. THE EFFECT OF HAVING A NON-TIGHT CONSTRUCTION OF THE DC-LINK

A non-tight construction of the dc-link is a source of disturbance. The system suffering interference is very small. The victim system is situated in the near-field region of the source system causing crosstalk. There are three types of crosstalk: common impedance coupling, capacitive coupling, and inductive coupling. In many situations crosstalk occurs as a mixture of common impedance and Electromagnetic field coupling.

A cable of 1m length was connected with the coaxial contact on the circuit board simulating a non-tight construction. The latter one causes oscillations in the output signal because the cable introduces an extra inductance in the circuit. The extra inductance, the inductance of the transformer and the capacitances of the MOSFET form a resonant circuit. Since the resonant frequency is given by

$$= \frac{1}{2\sqrt{LC}} \quad (10)$$

the higher inductance will reduce the resonance frequency and thereby shifting it below the switching frequency f_s and causing high frequency disturbances. The current at turn-off is forced to continue flowing through the extra inductance charging the capacitances of the MOSFET. This causes high frequent oscillations (Fig. 8) in the voltage as well as in the current. For comparison the waveforms of the previous configuration are shown in Fig. 9.

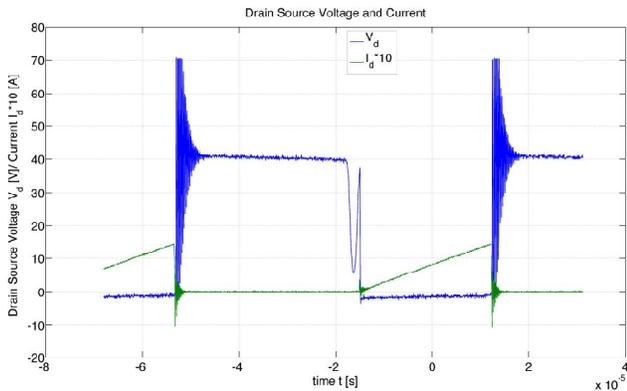


Fig. 8: Drain-source voltage and current with oscillations

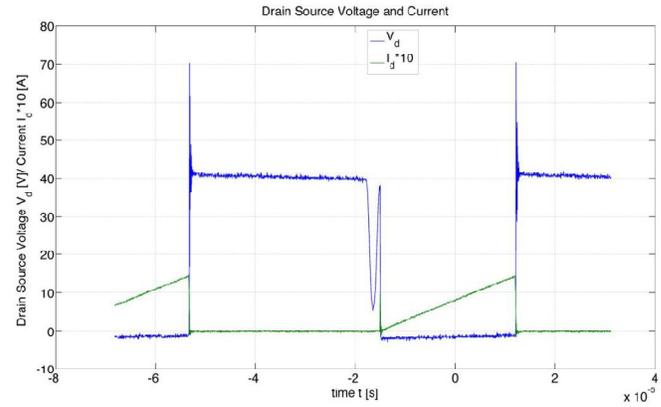


Fig. 9: Drain Source voltage and current before adding cable

In the Fig.9, it can be observed that oscillations appear in the turn-off of the MOSFET. These oscillations are to be avoided because they increase the stress in the switching device generating a larger power loss and thus decreasing its lifetime.

TABLE 3
COMPARISON OF POWER LOSSES W/ AND W/O EXTRA CABLE

	P_{ave} [W]	P_{cond} [W]	P_{on} [W]	P_{off} [W]	$I_{d,rms}$ [A]
Measurement w/o cable	0.692	0.4216	0.410	0.0113	0.607
Measurement w/ cable	0.832	0.632	0.601	0.0237	0.613
Deviation (%)	+20	+49	+46	+119	+1

Table 3 shows how remarkable the losses increased in comparison with those from the previous setup. The switch-off losses $P_{switch-off}$ are more than twice as high as before.

IV. THE EFFECT OF SNUBBER CIRCUIT TO DAMPING OSCILLATION

Apart from the undesirable increased losses during switch-off the oscillations might cause unacceptable electro-magnetic interference (EMI). To overcome these, a turn-off snubber is implemented. The circuit for such a device is presented in Fig. 10: Principal of turn-off snubber (surrounded red) Fig. 10 below.

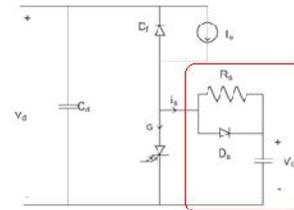


Fig. 10: Principal of turn-off snubber (surrounded red)

The capacity of the snubber circuit C_s takes the energy that is stored in the inductances away at turn-off and releases it at turn on. The aforementioned oscillations are in a manner of speaking "short-circuited" because the snubber capacity is relatively large compared to the MOSFET capacitances.

Although the following derivations present the procedure of designing a snubber that reduces the losses at turn-off and not primarily the reduction of EMI, the calculation give an idea of the range for the size of the snubber components.

From Fig. 10 above it can be seen that the current through a valve component is:

$$= 1 - \frac{t_{fi}}{t_{on}} \quad (11)$$

where t_{fi} is the fall time for the current i_G at turn off. The current is through the snubber is given as follows:

$$= \frac{V_d}{R_s} = \frac{V_d}{R_s} \quad (12)$$

The Capacitor C_s is charged with that current:

$$= \frac{V_d}{R_s} * C_s \quad (13)$$

The valve component has a reverse recovery current I_{rr} and the maximum discharge current for the snubber circuit is $I_{S,max}$, hence the maximum current flowing through the valve is:

$$= I_{rr} - I_{S,max} \quad (14)$$

I_{rr} should be about $0.2I_o$ according to [8].

In order to limit this current, the snubber resistance R_s should have the following value:

$$= \frac{V_d}{I_{rr} - I_{S,max}} \quad (15)$$

The capacitance has to be discharged before the valve is turned off again to be able to relocate the energy from the inductances. The following Equation is taken from the textbook [1].

$$2.3 \quad (16)$$

If Equation (16) is fulfilled the voltage over the capacitor is equal or below 10% of its maximal value. The capacitor energy dissipated in the snubber resistance during turn on is given by the equation:

$$= \frac{1}{2} C_s V_d^2 \quad (17)$$

And the power loss in the snubber circuit is:

$$= \frac{1}{2} C_s V_d^2 f \quad (18)$$

The total losses of the MOSFET and snubber combination consist of the transistor losses and the losses in the snubber resistance (assuming negligible losses in the snubber diode and capacity).

With (14) and (15) the snubber resistance was calculated. Proceeding with (16) results in a snubber capacitance $C_s = 40\text{nF}$, which seems to be the range since the capacitance of the MOSFET lie in the piko-region and C_s should be much larger. Simulating with different values for C_s and R_s in the PSpice model the best damping could be obtained with $R_s = 20 \Omega$ and $C_s = 22\text{nF}$. Following phenomena could be observed: With too high $R_s = 200 \Omega$ the oscillations were fairly high, but the voltage peak was reduced. Slightly increasing C_s has the same effect since the snubber diode has a finite resistance C_s is charged by a current flowing through both, which explains the high oscillations due to limited current flow. Best visually evaluated results were achieved with the first mentioned values. With those values the snubber is within the stated limitations in the equations.

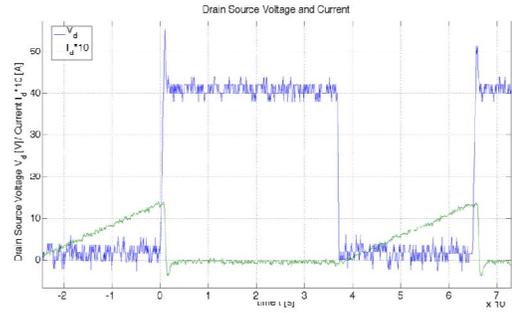


Fig. 11: Drain Source voltage and current after adding snubber Comparing the waveforms shown in Fig. 11 with those in Fig. 8 the oscillations have obviously been reduced.

V. CONCLUSIONS

The comparison of properties the fly-back converter for electric traction drives is simulated and measured. The change of DC-link has effect in efficiency of fly-back converter. The short dc cable have a good efficiency compare to long DC cable about 20%. The damping oscillation can be reduced by change the snubber circuit of MOSFET.

VI. REFERENCES

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